## DIVISIONAL APPLICATION TRANSMITTAL

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This is a request for filing a divisional application pursuant to 37 C.F.R. § 1.53(b), of pending prior application:

Serial No. 08/911,505 filed August 14, 1997, by Hidenori Ogata, Ken Wakita, Kiyoshi Yoneda, Yoshihiro Morimoto, Tsutomu Yamada, Kazuhiro Imao and Takashi Kuwahara (inventors currently of record in prior application) for Laser Anneal Method of a Semiconductor Layer.

1.  ☒  Enclosed is a copy of the prior application, including the oath or declaration as originally filed, or a replacement specification which does not add new matter.

2.  ☒  The filing fee is calculated below:

CC154312.1
005586D8326
04/13/1999 iy

## CALCULATION OF FEES

| ITEM | | TOTAL NO. OF CLAIMS | | NO. OF CLAIMS OVER BASE | LG/SM $ ENTITY FEE | | $ AMOUNT | $ FEE |
|---|---|---|---|---|---|---|---|---|
| A | TOTAL CLAIMS FEE | 3 | -20 | 0 | LG=$18 SM=$9 | $18 | 0 | |
| B | INDEPENDENT CLAIMS FEE* | 1 | -3 | 0 | LG=$78 SM=$39 | $78 | 0 | |
| C | SUBTOTAL - ADDITIONAL CLAIMS FEE (ADD FINAL COLUMN IN LINES A + B) | | | | | | | $ 0 |
| D | MULTIPLE-DEPENDENT CLAIMS FEE | | | | LARGE ENTITY FEE = $260 SMALL ENTITY FEE = $130 | | | $ 0 |
| E | BASIC FEE | | | | LARGE ENTITY FEE = $760 SMALL ENTITY FEE = $380 | | | $ 760 |
| F | TOTAL FILING FEE (ADD TOTALS FOR LINES C, D, AND E) | | | | | | | $ 760 |
| | *LIST INDEPENDENT CLAIMS  9 | | | | | | | |

3. ☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Account No. 12-1820. A copy of this sheet is enclosed.

4. ☒ A check in the amount of $760 is enclosed.

5. ☒ Cancel in this application original claim(s) 1-8 of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

6. ☒ Amend the specification by inserting before the first line the sentence:

This is a division of application Serial No. 08/911,505 filed August 14, 1997, which application is hereby incorporated by reference in its entirety.

7a. ☐ New formal drawings are enclosed.
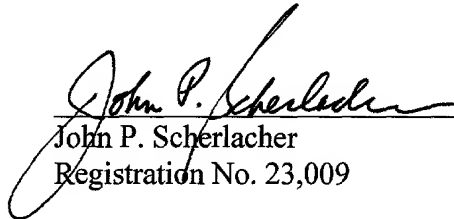
7b. ☒ Priority of application Serial Nos.:

Japanese application Serial No. Hei 8-217424 filed August 19, 1996 is claimed under 35 U.S.C. § 119.

7c. ☒ The certified copy of the priority application has been filed in prior application Serial No. 08/911,505, filed August 14, 1997.

8. ☒ The prior application is assigned of record to:  Sanyo Electric Co., Ltd.

9. ☒ The power of attorney in the prior application is as listed on the attached copy of the declaration filed in the patent application.

    a. ☒ The power appears in the original papers in the prior application.

    b. ☐ Since the power does not appear in the original papers, a copy of the power in the prior application is enclosed.

c. ☒ Address all future communications to:

John P. Scherlacher
LOEB & LOEB LLP
10100 Santa Monica Blvd., 22nd Floor
Los Angeles, CA 90067-4164
310-282-2000

10a. ☐ A preliminary amendment is enclosed. (Claims added by this amendment have been properly numbered consecutively beginning with the number next following the highest numbered original claim in the prior application.)

10b. ☐ A separate check for $___ is enclosed to cover additional claims added by the preliminary amendment.

11. ☐ Enclosed find the following declaration(s) in support of Small Entity status for this application:

     ☐ Inventor(s)
     ☐ Individual other than inventor
     ☐ Nonprofit organization
     ☐ Small business concern

12. ☐ The statement(s) of Small Entity Status filed in the prior application is (are) still proper.

Date: April 14, 1999

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PATENT
Attorney Docket No: 005586/D8326

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re divisional application of:

Hidenori Ogata et al.

Parent Serial No:     08/911,505

Parent Filed:     August 14, 1997

For:     Laser Anneal Method of a Semiconductor
Layer

Art Unit:     2822

Examiner:     M. Wilczewski

CERTIFICATE OF MAILING VIA U.S. EXPRESS MAIL
"Express Mail" Mailing Label No. EL225776714US
Date of Deposit: April 14, 1999

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I hereby certify that

☒     two copies of a letter of divisional application transmittal

☒     check in amount of $ 760 as filing fee

☒     a copy of parent patent application as filed ( 40 page(s) of specification; 11 claim(s); 1 page(s) of abstract

☒     25 sheet(s) of informal drawings

☒     executed Declaration and Power of Attorney as filed in the parent applicaiton

☐     Verified Statement (Declaration) Claiming Small Entity Status

☐     certified copy of ___ patent application No. ___ which was filed___ from which priority is claimed in the subject case pursuant to 35 U.S.C. § 119

☐     Preliminary Amendment

☒     Information Disclosure Statement with 14 references

☒     return postcard

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service with sufficient postage under 37 C.F.R. § 1.10 on the date indicated above and are addressed to:

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231.

Date: April 14, 1999

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Mary Warren
Name of person mailing papers

_Mary Warren_
Signature

CC193081.1
005586D8326
04/13/1999 iy

EL225776714US

## TITLE OF THE INVENTION

## LASER ANNEAL METHOD OF A SEMICONDUCTOR LAYER

## BACKGROUND OF THE INVENTION

5      FIELD OF THE INVENTION

The present invention relates to a method for manufactur-
ing a semiconductor device, particularly to a method for
manufacturing an LCD (liquid crystal display) such as a driver
circuit integrated type LCD in which TFTs (thin film transis-
10     tors) comprising a polycrystal semiconductor layer are formed
in a display area and a driver area.

DESCRIPTION OF THE RELATED ART

In recent years, LCDs have been regularly employed in OA
15     and AV apparatuses because of advantages resulting from their
small size and thickness and their low power consumption.
Active matrix type displays, in which each pixel is equipped
with a TFT as a switching device for controlling the rewrite
timing of image data, are especially able to display moving
20     pictures with high resolution on a large screen, and are
therefore used for displays in various televisions, personal
computers, and the like.

A TFT is an FET (field effect transistor) obtained by
forming a semiconductor layer together with a metal layer in a
25     predetermined shape on an insulating substrate.  In an active
matrix type LCD, each TFT is connected to an electrode of each
pixel capacitor formed between a pair of substrates, for

driving liquid crystal.

In particular, developments have been made to LCDs using polycrystal silicon (p-Si) as a semiconductor layer in place of amorphous silicon (a-Si) which has previously been common, and annealing with use of a laser beam has been put to use for formation or growth of crystal grains of p-Si. In general, p-Si has a higher mobility than a-Si so that using p-Si to form a TFT can downsize TFTs, allowing a high aperture ratio and a high resolution to be realized. In addition, since TFTs can be constructed in a gate self-alignment structure, fine TFT elements can achieve higher speed operation by reductions in parasitic capacity. By using these TFTs to form an electric complementary connection structure between an n-ch TFT and a p-ch TFT, i.e., a CMOS, a higher speed driver circuit can be constructed. Therefore, a driver circuit section can be formed to be integrated with a display pixel section on one substrate, allowing manufacturing costs to be reduced and realizing a small size LCD module.

Known methods of forming a p-Si layer on an insulating substrate include a crystallization method under a high temperature, by annealing a-Si formed under a low temperature, a solid phase crystallization method under a high temperature, and the like. In all known methods, some treatment must be carried out under a high temperature of 900℃ or more. Therefore, it is not possible to use a low cost non-alkaline glass substrate as an insulating substrate in view of heat resistance and, as quartz glass substrate is required, a

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higher manufacturing cost results. In contrast, developments have been made to a method which allows use of a non-alkaline glass substrate as an insulating substrate by performing silicon polycrystallization processing at a relatively low

5      substrate temperature of 600°C or less, through use of laser annealing. Such processes, in which the processing temperature is 600°C or less throughout all TFT manufacturing steps are called "low-temperature processes", and are essential for mass-production of low cost LCDs.

10     FIG. 1 shows a state of a substrate to be processed by excimer laser annealing (hereinafter referred to as "ELA"). A substrate 1 to be processed is a popular non-alkaline glass substrate. An a-Si layer is formed on the surface of the substrate 1. An active matrix substrate 5 is a substrate for

15     constructing an LCD comprising a display area 2 where display pixels are arranged in matrix, and a gate driver 3 and a drain driver 4 provided surrounding the display area 2. The substrate 1 is a mother glass substrate including a plurality of active matrix substrates 5. In the display area 2, pixel

20     electrodes, each being an electrode of a pixel capacitor for driving liquid crystal, are formed and arranged in matrix, and are respectively connected with TFTs formed. The gate driver 3 is mainly constructed by a shift register, and the drain driver 4 is mainly constructed by a shift register and a

25     sampling circuit. These drivers are formed by a TFT array such as a CMOS or the like.

Each of TFTs is formed such that, as shown in FIG. 2, a p-

Si layer obtained by crystallization of an a-Si layer by use of the ELA method is used as an active layer. In the area where a p-Si layer 11 etched into an island-like shape is formed, a non-doped channel region CH, light-doped regions LD,

5    and heavy-doped source and drain regions S, D are arranged. On the channel region CH, a gate electrode 13 is arranged with a gate insulating film interposed between the channel region and the gate electrode 13. A source electrode and a drain electrode are connected to the source and the drain regions

10    respectively. In the driver circuit areas, a TFT is connected to form a CMOS or the like. In a display area, a signal line and a pixel electrode are connected to the respective drain electrode and the source electrode.

As shown in FIG. 1, in a conventional laser annealing

15    method, a line beam is irradiated on a substrate 1 such that the contour of edge lines C of a band-like irradiated region of a line beam irradiated on the substrate 1 is shifted by a predetermined overlap amount. Scanning is carried out as indicated by the arrow in the drawing, and the entire

20    substrate is subjected to annealing. However, after scanning is thus performed with a line beam, there remains a defective crystallization region in which sufficient crystallization was not attained and grains with a smaller grain size, as indicated by reference R in the figure, remain in p-Si formed.

25    This region is formed in a fine liner shape along the longitudinal direction of the irradiated region, and appears in a striped pattern. Since this defective crystallization

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region R has a low mobility and a high resistance, the
characteristics of TFTs formed in this region are degraded.
If the characteristics of TFTs are thus degraded, pixel
capacitors are not sufficiently charged in the display area so
that the contrast ratio is lowered, or erroneous operation is
caused in the driver circuit area, thus disadvantageously
influencing display.

It is estimated that a defective crystallization region as
described above is caused because of unevenness in energy of
an irradiated laser beam. Laser annealing strongly depends on
the energy of the irradiated laser beam. In general, the
grain size of crystal tends to increase as the irradiation
energy increases. However, when the energy level increases to
a certain level Eu or more, the grain size rapidly decreases
to the microcrystal level. Hence, it is demanded that the
energy level of a laser beam to be irradiated onto an a-Si
layer should be as large as possible within a range of Eu to
Ed which is lower than an upper limit level Eu such that the
energy level does not exceed the upper limit Eu, in order to
enlarge the grain size as much as possible thereby to achieve
TFTs having excellent characteristics.

FIG. 3 shows an energy distribution of an irradiation beam
with respect to positions in a line beam. An optical system
for generating a line beam is provided with a line width
adjust slit and a line length adjust slit, to form a line beam
of a band-like or rectangular shape. Thus, since the line
width A of the line beam is defined by the line width adjust

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slit, the characteristic curve of the irradiation light intensity distribution has substantially sharp edges and a substantially flat energy distribution peak portion Eo, as shown in FIG. 3. However, in regions X and B in FIG. 3, the energy level is extremely high or low and is thus greatly differs from the level at the flat portion.

In an optical system comprising a plurality of lenses, light is diffracted or interfered due to slight concave and convex portions existing in the lens surfaces or foreign material contamination or the like adhering thereto. The light thus diffracted or interfered is converged in the line width direction A and is expanded in the line length direction, so that nonuniformity of energy of the laser beam irradiated toward the substrate 1 from the optical system is increased. Even slight amounts of foreign material or the like present in a clean room, may cause nonuniformity in light intensity. Therefore, nonuniformity of the output energy of a line beam cannot be completely eliminated at present, and it is unavoidable that the energy level of a line beam to be irradiated partially exceeds the upper limit which allows an appropriate grain size.

As a result of this, a line beam whose energy level is uneven is intermittently irradiated as shown in FIG. 3, and a laser beam which partially exceeds the upper limit Eu of the energy level is irradiated within a unit irradiated region having edge lines C as shown in FIG. 1. It is therefore considered that a much finer linear defective crystallization

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region R is caused within the edge lines C.

## SUMMARY OF THE INVENTION

The present invention has an object of providing a method of preventing nonuniformity in semiconductor layer characteristics and of obtaining a semiconductor layer with excellent characteristics by means of laser anneal processing.

To achieve the above object, the present invention provides a laser anneal method for improving quality of a semiconductor layer formed on a substrate by irradiating a laser beam or for obtaining a polycrystal semiconductor layer from an amorphous semiconductor layer, wherein an energy level of the laser beam in a region to be irradiated is set such that a level towards the rear of the region along which the laser beam scans is lower than that at the front area or the center area of the region.

Thus, after a high energy part of the laser beam at a relatively forward part with respect to the scan direction passes through the semiconductor layer, a lower energy part passes through the semiconductor layer sequentially. Therefore, after large crystal grains are initially formed by the high energy part, remaining defective crystallization regions are crystallized by the relatively low energy part while the large crystal grains are maintained, thereby improving crystallinity for the entire region.

In another aspect, the present invention provides a laser anneal method of a semiconductor layer for obtaining a

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polycrystal semiconductor layer by irradiation of an amorphous semiconductor layer formed on a substrate with a laser beam, wherein an energy level at a region to be irradiated by the laser beam is set such that the peak level in the rear area of the region along a scan direction of the laser beam is lower than the upper limit the energy level that maximizes the semiconductor layer grain size.

Thus, the irradiated energy does not exceeds the upper limit energy level which maximizes the grain size at the rear area of the irradiated laser beam along the scan direction passing over the amorphous semiconductor layer sequentially, therefore it is possible to prevent the semiconductor layer from being changed into an amorphous state, and to carry out crystallization with defective crystallization regions. Accordingly, a polycrystal semiconductor layer having an almost uniform grain size over the entire region of the semiconductor layer can be formed.

In a further aspect, in addition to the above-described condition, the peak level of the laser beam at the front area or the center area of the region is substantially equal to or more than the upper limit energy level which maximizes the grain size of the semiconductor layer.

In yet another aspect of the present invention, the upper limit energy level which maximizes the grain size of the semiconductor layer is corresponds to the lower limit energy level over which the polycrystal semiconductor layer is changed into an amorphous state.

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Thus, the level of the irradiated laser beam passing over the semiconductor layer exceeds the upper limit energy level in some cases because the energy level at the front area ·is relatively high, allowing the semiconductor layer to be

5    microcrystallized by such a laser beam.  However, the energy level irradiated to the semiconductor layer gradually decreases as the laser beam scanning proceeds from the front area to the rear area because the energy level is set such that a level at the rear area is lower than that at the front,

10   which allows the energy level irradiated to the semiconductor layer to not exceed the upper limit energy level and to yet be sufficiently high and optimal.  The latter half of the laser annealing process for a predetermined region of the semiconductor layer is performed in an energy range in which a

15   sufficiently large grain size can be formed by employing such an energy profile of the laser beam, because an energy range which is optimal to maximize the grain size is just below the upper limit.  Therefore, the laser anneal processing is performed under the best conditions.  As a result, a

20   polycrystal semiconductor layer with a large grain size and excellent uniformity is formed.

   According to another aspect of the present invention, the laser beam irradiated on the amorphous semiconductor layer is obtained by shaping a laser beam generated from a laser

25   oscillation source by an optical system including a plurality of lenses, such that the region to be irradiated has a predetermined shape, and the energy level, energy

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distribution, or their combination in the region to be irradiated by the laser beam is controlled by adjusting a distance between the amorphous semiconductor layer formed on the substrate and the focal point of the laser beam formed by the optical system.

By thus controlling the distance between the substrate on which the amorphous semiconductor layer is formed and the focal point of the laser beam formed by the optical system, the energy profile of the laser beam is easily modified in a desired shape, thereby allowing a better laser anneal processing to be performed by a simple control.

According to yet another aspect of the present invention, the scan direction of the laser beam is set such that an energy level at the rear area of the region along the scan direction is lower than the upper limit energy level, which allows the laser profile along the scan direction to be more simple and suitable.

In another aspect, the present invention is a transistor device in which a polycrystal semiconductor layer is formed by subjecting an amorphous semiconductor layer formed on a substrate to laser anneal processing, wherein an energy level in a region to be irradiated by a laser beam of the amorphous semiconductor layer is set such that the level at the rear area of the region along a scan direction of the laser beam is lower than the upper limit energy level which maximizes a grain size of the semiconductor layer, and the amorphous semiconductor layer is annealed by the laser beam and the

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polycrystal semiconductor layer obtained is used as an active layer of the transistor device.

According to yet another aspect of the present invention of the transistor device, the transistor device is a thin film transistor, and a channel layer of this thin film transistor is formed in the polycrystal semiconductor layer obtained by the laser anneal processing.

In a further aspect of the present invention, the transistor device is a thin film transistor, a channel layer of this thin film transistor is formed in the polycrystal semiconductor layer obtained by the laser anneal processing, and the thin film transistor is used as a switching device formed in a display area of a substrate forming a liquid crystal display and as a switching device of a driver circuit formed surrounding the display area of the substrate through a process substantially equal to a process of forming the switching device of the display region.

By thus controlling the laser energy to form a polycrystal semiconductor layer and by using the layer as an active layer of a transistor device, for example a thin film transistor, it is possible to obtain a transistor device with a high speed and excellent characteristics. Further, since a polycrystal semiconductor layer having excellent characteristics is obtained, it is possible to form a transistor device having a gate-self-align structure. If this kind of transistor is used as a switching device of a display area and as a switching device of a driver circuit area for driving the switching

device of the display area in the liquid crystal display or the like, it is possible to form a display with excellent display quality.

## BRIEF DESCRIPTION OF THE DRAWINGS

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FIG. 1 is a view explaining a conventional positional relationship between a substrate to be processed and a region to be irradiated by a line beam.

FIG. 2 is a view showing a planar construction of a TFT

10　formed by a conventional laser anneal.

FIG. 3 is a graph explaining an energy profile of an irradiation laser beam.

FIG. 4 is a view explaining a positional relationship between a substrate to be processed and a region to be

15　irradiated by a line beam according to an embodiment of the present invention.

FIGs. 5, 6, 7 and 8 are graphs explaining an energy profile of a line beam according to an embodiment of the present invention.

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FIG. 9 is a graph showing a relation between laser beam irradiation time (the number of pulse shots) and temperature of a film to be processed in the ELA according to an embodiment of the present invention.

FIG. 10 is a graph showing a relation between laser beam

25　irradiation time (the number of pulse shots) and a grain size of a film to be processed in the ELA according to an embodiment of the present invention.

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FIG. 11 is a view showing a correlation between beam profile and state of a film to be processed in an ELA according to an embodiment of the present invention.

FIG. 12 is a view showing a correlation between a beam profile, a state of a film, a position in the film, and a grain size at a timing in the ELA according to an embodiment of the present invention.

FIGs. 13A, 13B and 13C are views showing microphotographs showing the view of the state of a film shown in the middle section of FIG. 12.

FIG. 14 is a view showing a correlation between beam profile and state of a film to be processed in an ELA according to an embodiment of the present invention.

FIG. 15 is a view showing a correlation between a beam profile, a state of a film, a position in the film, and a grain size at a timing in the ELA according to an embodiment of the present invention.

FIGs. 16A, 16B and 16C are views showing color microphotographs showing the state of a film shown in the middle section of FIG. 15.

FIG. 17 is a graph showing a relation between laser energy and grain size in an ELA according to an embodiment of the present invention.

FIG. 18 is a schematic view of the structure of a laser irradiation apparatus used in an embodiment of the present invention.

FIGs. 19 and 20 are views explaining the structure of an

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optical system of a laser irradiation apparatus shown in FIG. 18.

FIG. 21 is a graph showing a beam profile of a laser beam used in an ELA according to Example 1 of the present invention.

FIGs. 22A, 22B and 22C are views showing microphotographs of a p-Si layer when the scan direction of a laser beam shown in FIG. 21 is set in the left direction in FIG. 21.

FIGs. 23A, 23B and 23C are views showing microphotographs of a p-Si layer, when the scan direction of a laser beam shown in FIG. 21 is set in the right direction in FIG. 21.

FIG. 24 is a graph showing a beam profile of a laser beam used in an ELA according to Example 2 of the present invention.

FIGs. 25A, 25B and 25C are views showing microphotographs of a p-Si layer when the scan direction of a laser beam shown in FIG. 24 is set in the left direction in FIG. 24.

FIGs. 26A, 26B and 26C are views showing microphotographs of a p-Si layer when the scan direction of a laser beam shown in FIG. 24 is set in the right direction in FIG. 24.

FIG. 27 is a graph showing a beam profile of a laser beam used in an ELA according to Example 3 of the present invention.

FIGs. 28A, 28B and 28C are views showing microphotographs of a p-Si layer when the scan direction of a laser beam shown in FIG. 27 is set in the left direction in FIG. 27.

FIGs. 29A, 29B and 29C are views showing microphotographs

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of a p-Si layer when the scan direction of a laser beam shown in FIG. 27 is set in the right direction in FIG. 27.

FIG. 30 is a view showing a planar construction of a TFT formed by a laser anneal according to an embodiment of the present invention.

FIG. 31 is a view schematically showing a cross-section of the structure of the TFT shown in FIG. 30.

FIG. 32 is a view schematically showing a cross-section of the structure of a display area in a liquid crystal display apparatus using a TFT according to an embodiment of the present invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 4 is a plain view for showing a state of a substrate to be processed by an ELA according to an embodiment of the present invention. The substrate 7 to be processed is a popular non-alkaline glass substrate, and an a-Si layer is formed on its surface. An active matrix substrate 25 forms one substrate of an LCD comprising a display area 22 where display pixels are formed and arranged in matrix, and a gate driver 23 and a drain driver 24 formed and arranged surrounding display area 22. The substrate 7 is a mother glass substrate including six active matrix substrates 5. In the display area 22, pixel electrodes, each being an electrode of a pixel capacitor for driving liquid crystal, are arranged in matrix and each TFT is formed to be connected with each respective pixel electrode. The gate driver 23 is mainly

constructed by a shift register, and the drain driver 24 is

mainly constructed by a shift register and a sampling circuit.

These drivers are formed by a TFT array such as a CMOS or the

like, and each TFT is formed with use of p-Si formed by the

5    ELA method according to the present invention, as a channel

and a source/drain layer.

In an embodiment of the present invention, ELA is

performed by irradiating a line beam obtained from a laser

irradiation apparatus, as will be described below, onto a

10   substrate 7 as a substrate to be processed, to scan the

substrate with the beam.  An excimer laser is a pulse laser,

and a line beam of the pulse laser is intermittently

irradiated onto the substrate 7 to be processed such that the

substrate 7 is scanned in the direction indicated by the arrow

15   in FIG. 4 (corresponding to the longitudinal direction in the

figure) with the line beam.  Further, the line beam is

controlled such that irradiated regions of any successive

pulse beams overlap each other by a predetermined amount (See

edge lines C in the figure.)  The entire surface of an

20   amorphous semiconductor layer on the substrate 7 is annealed

by scanning the substrate 7 while thus sequentially shifting

the position of the line beam to be irradiated.

A line beam generated by a laser irradiation apparatus, to

be described below, has an approximate line length of 80 to

25   300mm and a line width of 0.1 to several mm.

Scanning is performed such that the line beam is moved as

described above in the line width direction on the substrate

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7, and is carried out for each active matrix substrates 25
arranged in a plurality of columns (e.g., in two columns in
FIG. 4) on the substrate 7 to be processed as a mother
substrate.  In this manner, annealing is performed once on the

5      entire surface of the substrate 7 to be processed.

An energy profile of a line beam, according to the present
embodiment, for obtaining polycrystal silicon with a
preferable grain size is next explained referring to FIGs. 5
to 8.  The present embodiment is based on the fact that a

10     final grain size of a film is influenced by an energy level at
the latter half of the laser anneal processing, and employs a
line beam having an energy profile suitable for an annealing
process in an energy range which maximizes the grain size.

FIGs. 5 to 8 are energy profiles devised from such a point

15     of view, and each of the figures shows a relation between a
position of a irradiated line beam (a sheet beam) along the
line width direction and an energy level.  FIG. 5 is an
example where a beam profile is shaped in a trapezoid in which
a level at the front area with respect to the scan direction

20     is different from the rear area.  FIG. 6 is an example where
an edge of a beam profile shaped in a trapezoid is shaded off.
FIGs. 7 and 8 are examples of cases where that beam profiles
are not as clearly defined as in FIGs. 5 and 6.  In all of the
examples, the energy level exceeds the threshold value energy,

25     Eth, over which a silicon grain is microcrystallized in a line
beam area corresponding to the front area along a scan
direction of the line beam, i.e., the front area along the

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line width direction. However, the energy profile has a shape

that the energy level does not exceed the threshold value

energy Eth in the backward area relative to the front area.

Therefore, it is possible to anneal an amorphous silicon in an

5     energy range GR which is optimal for obtaining a sufficiently

large grain size and exists just below the threshold value

energy Eth, which allows the laser anneal processing for

crystallization to be performed in the optimal conditions.

       FIG. 9 shows a relation where crystallinity depends on a

10    film temperature when a laser beam is irradiated. Temperature

is measured by a well-known crystal lattice state optical

observation method, such as a method using a pyrometer, and

relates to energy of the ELA. In this figure, a manner of

crystallization of an a-Si layer as a starting film is shown.

15    According to this manner, the film temperature rises as time

passes after irradiation begins, and the film temperature

falls after irradiation stops. With regard to the curve "a"

in the figure, the maximum attainment point of the film

temperature does not exceed the polycrystallizing temperature

20    Tg, therefore, even after the irradiation ends, the film

temperature being lowered and crystallization being inactive,

the state of the a-Si layer is maintained as it is. With

regard to the curve "b", the maximum attainment point of the

film temperature exceeds the polycrystallizing temperature Tg,

25    therefore, after irradiation ends, the film temperature is

lowered and crystallization is inactive, and a p-Si(S) film

with small size grains is formed. With regard to the curve

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"c", the maximum attainment point of the film temperature is higher than the curves "a" and "b", therefore, a p-Si(L) film with large size grains is formed. With regard to the curve "d", the film temperature exceeds the polycrystallizing

5      temperature Tg and the microcrystallizing temperature TM over which a grain size becomes small, therefore, after irradiation ends, film temperature is lowered and crystallization becomes inactive, causing a microcrystalline silicon (M-cry) film to form. The difference of "a", "b", "c", and "d" is caused by

10     ELA energy. Accordingly, it is understood that the film temperature should be raised as high as possible such that the temperature does not exceed the microcrystallizing temperature TM, for obtaining a p-Si(L) film having large grain size and satisfactory annealing.

15     FIG. 10 shows a relation between irradiation time, specifically the number of irradiated laser pulse shots, and grain size. The grain size increases as the number of pulse shots and an ELA energy increase, in a condition that the film temperature is equal to or less than the microcrystallizing

20     temperature TM shown in FIG. 9. The grain size rapidly increases over the initial several shots, and gently increases by the succeeding shots.

This ELA property was derived from experimental results as described below.

25     A p-Si layer formed by the ELA with relatively high energy, as will be described in detail later, was first Secco etched. Its film state was then examined using an SEM, an

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optical microscope, and other means.  As a result, an ELA

property as shown in FIG. 11 was found.  The upper section of

the figure is a beam profile showing a relation between laser

irradiation position and energy, wherein the horizontal axis

5    [Position] refers to a position along the width direction of a

line beam or a scan direction of the beam, and the vertical

axis [Temperature] refers to film temperature, having a

relation to the laser energy, measured by optical observation

of a lattice state.  The lower section of the figure is a view

10   showing a layer state, processed by the ELA, corresponding to

the beam profile.  The beam profile is shaped in a trapezoid

in which the temperature level at the top of the profile

exceeds the microcrystallizing temperature TM, therefore a

film corresponding to the top is in a microcrystal (M-cry)

15   state.  At the sides of the trapezoidal profile having a steep

slope with a straight line or a smooth curved line, the film

temperature rises and exceeds the polycrystallizing

temperature Tg and the microcrystallizing temperature TM, as

nearer the central part of the region to be irradiated by the

20   laser beam along the width direction, the top of the

trapezoidal profile, or the microcrystal region.  The most

outer part of the film corresponding to the temperature region

equal to or less than the polycrystallizing temperature Tg of

the beam profile is in an a-Si state, and the film

25   corresponding to the temperature region from the

polycrystallizing temperature Tg to the microcrystallizing

temperature TM is in a p-Si state.  A grain size of p-Si

20

successively increased from the a-Si region, as the film

temperature increased over the polycrystallizing temperature

Tg shown in the profile. The most characteristic point was

that the grain size increased according to temperature until

5    temperature attained the microcrystallizing temperature TM,

and then grain size rapidly decreased to be changed into

microcrystal over the microcrystallizing temperature TM. As a

result, the maximum grain size was obtained at the highest

temperature region MX which does not exceed the

10   microcrystallizing temperature TM.

FIG. 12 is a view explaining a state of a processed film

obtained by scanning a line beam having an energy profile as

shown in FIG. 11 on the a-Si layer. The upper section of FIG.

12 is an energy profile of a laser beam identical to FIG. 11,

15   the middle section of FIG. 12 is a schematic view of a state.

of the processed film obtained by laser annealling, and the

lower section of FIG. 12 shows a relationship, connected with

the middle section, between a film position corresponding to

the processed film in the middle section along beam scan

20   direction and grain size. FIG. 12 shows that an irradiated

position is at the position shown in the figure as the beam

proceeded while the irradiated position was sequentially

shifted from the left side of FIG. 12. In this experiment, a

scan of the line beam was set such that each laser pulse 95%

25   overlapped each next pulse and twenty laser pulses were

repeatedly scanned for a unit irradiated region in one

instance. FIG. 13A is an optical microphotograph

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(magnification: x125) of the processed film which is a base of the schematic view of a state of the film shown in the middle section of FIG. 12. FIG. 13B is an optical microphotograph (magnification: x250) enlarging the left side region of FIG.

5    13A. FIG. 13C is an optical microphotograph (magnification: x250) enlarging the right side region of FIG. 13A.

In each laser pulse, p-Si of a sufficiently large grain size GM was sequentially formed at a film corresponding to the MX region that is an edge part of the beam profile, while M-

10   cry was formed at a temperature region over the temperature TM at the front area of the MX region of the energy profile with respect to the scan direction, thereby forming a striped pattern. In other words, it is understood that while M-cry formed by previous pulses is crystallized by succeeding

15   pulses, fine linear p-Si is formed in the film region corresponding to the temperature region MX for obtaining the maximum grain size GM while in other regions, an energy level by which a grain size of M-cry can be more increased is not given. There is also an MX region for obtaining a

20   sufficiently large grain size at a front edge part of the beam profile along the scan direction. However, M-cry is formed while the top of the beam profile thereafter passes through.

A p-Si layer formed by relatively low energy ELA, in which the peak energy level of a line beam was set such that it was

25   lower than the beam illustrated in FIG. 11, was Secco etched and its film state was examined using an SEM, an optical microscope, or the like, with a result as shown in FIG. 14.

22

The upper section of the figure is, as was the case in FIG. 11, an energy profile against an irradiation position of a laser beam along a scan direction, and the lower section of the figure is a view showing a state of a film processed by

5    ELA obtained by irradiating a laser beam with this beam profile. While the beam profile is trapezoid shaped as in FIG. 11, the energy level of the line beam is set relatively low, therefore its top did not exceed the microcrystallizing temperature TM, which allowed ELA to be performed at a

10   temperature region over the polycrystallizing temperature Tg. As a result, p-Si having a not very large grain size was formed. The state of a-Si was maintained in its prior state, under the polycrystallizing temperature Tg.

FIG. 15 is a view explaining a state of a processed film

15   obtained by scanning the line beam having the energy profile shown in FIG. 14 on an a-Si layer. The upper section of FIG. 15 is an energy profile of a laser beam identical to FIG. 14, the middle section of FIG. 15 is a schematic view of a state of the processed film obtained by laser annealling, and the

20   lower section of FIG. 15 shows a relation, corresponding to the number of laser shots, between a film position corresponding to the processed film in the middle section with respect to a scan direction of the beam and a grain size. FIG. 15 shows that an irradiated position is at the position

25   shown in the figure at a time, in a condition that the line beam proceeds while the irradiated position is sequentially shifted from the left side of FIG. 15. In this experiment, a

23

scan of the line beam was set such that each laser pulse 95%
overlapped each other pulse and twenty total pulses per scan
were repeatedly performed for a unit irradiated region. FIG.
16A is an optical microphotograph (magnification: x125) of the

5    processed film which is a base of the schematic view of a
state of the film shown in the middle section of FIG. 15.
FIG. 16B is an optical microphotograph (magnification: x250)
enlarging the left side region of FIG. 16A. FIG. 16C is an
optical microphotograph (magnification: x250) enlarging the

10    right side region of FIG. 16A. At the conditions shown in
FIGs. 15 and 16A to 16C, microcrystal was not formed by change
into an amorphous state, because laser energy did not exceed
the microcrystallizing temperature TM, which allowed
crystallization to proceed as the number of pulses increased,

15    thus enlarging the grain size.

An a-Si layer was crystallized by the initial four pulses
to change the grain size into Gg and the grain size further
gently increases as the number of pulses is increased.
Finally, the grain size attained to the maximum size Gp

20    obtained by ELA energy in this experiment at the 12th pulse.
A large change in the grain size was not observed thereafter.

The following information was revealed by the above
described experiments. In order to increase silicon grain
size by ELA, an increase of an energy level was required.

25    However, if an energy value exceeded a certain value, the
silicon returned to an amorphous state and grain size rapidly
decreased, thus forming microcrystal. Referring to FIG. 17,

24

which shows a relationship between ELA energy and grain size, the grain size increased as energy increased. The grain size attained its maximum when energy exceeded Ed at which a sufficiently large grain size GM could be obtained. Further

5    increases in energy decreased, and soon rapidly decreased, the grain size. While it was not proven that the energy level which maximizes the grain size strictly agrees with such threshold value energy, the energy level which maximized the grain size in the experiments was very close to the threshold

10   value energy and the threshold value energy was larger than the energy level which maximizes the grain size. Therefore, hereinafter, the energy level which maximize the grain size and the threshold value energy over which the grain size rapidly decreases are regarded to as identical for practical

15   purposes. In other words, it is defined that such threshold value energy is a border; the maximum grain size can be obtained just under the border and microcrystal is obtained over the border. Such threshold value energy is referred to as the upper limit Eu of the allowed area.

20       It is understood from FIG. 17 that an energy level should be in a range from Ed to Eu to obtain a grain size over GM. Particularly, it is understood from the shape of the characteristic curve in the figure that the laser energy should be as high as possible within a range under the

25   threshold value energy over which silicon is changed into an amorphous state to obtain maximum grain size. However, as shown in FIG. 3, unevenness of irradiated laser energy cannot

25

be avoided.  Therefore, when an irradiated energy exceeds, even slightly, the threshold value energy over which the grain size rapidly decreases the corresponding region becomes a defective crystallization region, thereby degrading

5    characteristics of a TFT formed in this region.

Accordingly, excellent ELA can be performed by an energy profile such that, as shown in FIGs. 5 to 8, the energy level gently decreases from the front side along the scan direction of an irradiated laser beam to the backside to intersect the

10    level of the threshold value energy Eth over which grain size rapidly decreases.  The energy level of the beam profile exceeds the threshold value energy Eth at the front area along the scan direction of the beam.  The level lowers as nearer the rear area with respect to the scan direction, allowing an

15    annealing with the maximum energy which does not exceed the threshold value energy Eth within the region GR just below the intersection of the energy Eth and the profile to be performed, thereby forming a p-Si layer having the maximum grain size.  In other words, there is an energy region GR,

20    which maximizes grain size, at just below the threshold value energy Eth over which a grain size rapidly decreases. Microcrystal is formed in a region having an energy level over the threshold value energy Eth at the front area  of the region GR.  Passing through the region GR next forms a p-Si

25    layer of maximum grain size.  In the region at the rear of the region GR, the grains, once formed, are never microcrystallized, since the energy level in this region does

not exceed the threshold value energy Eth. Accordingly, it is possible to form a p-Si layer of maximum grain size because of excellent annealing over the entire region of a film to be processed by setting an overlap amount and a pulse frequency such that an area in the film to be processed is shot at predetermined times within the region GR.

The structure of the above laser irradiation apparatus for performing laser annealing will next be explained with reference to FIG. 18.

In this figure, reference 51 denotes a laser oscillation source. References 52 and 61 denote mirrors. References 53, 54, 55, and 56 denote cylindrical lenses. References 57, 58, 59, 62, and 63 denote convergence lenses. A reference 60 denotes a slit determining the line width direction, and a reference 65 denotes a slit determining the line length direction. A reference.64 denotes a stage for supporting a substrate 7 to be processed which has a surface where an a-Si layer is formed. The slit 65 is provided close to the stage 64.

Laser light is supplied by an excimer laser in a pulse wave form. Laser light irradiated from the laser oscillation source 51 is shaped by two pairs of condenser lenses consisting of a pair of cylindrical lenses 53 and 55 and a pair of cylindrical lenses 54 and 56, into parallel light whose intensity has an almost flat output distribution in the longitudinal and lateral directions. This parallel light is referring to Fig. 19, converged in one direction by lenses 58,

59, 62, and 63, and is referring to Fig. 20, expanded in another direction by a lens 57, to create a band-like, rectangular, or linear for practical purposes, beam that is irradiated on the substrate 7 to be processed. A slit 60 for

5      adjusting the line width and a slit 65 for adjusting the line length respectively shield both end portions in the line width direction [A], and in the line length direction, to clearly define the shape to be irradiated, thus generating a line beam of a width A while constantly maintaining the intensity in the

10     effective irradiation region.

The stage 64 where the substrate 7 is mounted is arranged to be movable in the X- and Y-directions. With use of this kind of apparatus, the annealing processing as described above can be carried out with a high throughput for a substrate of a

15     large area, even when annealing processing is carried out in a plurality of steps.

In addition, the laser irradiation apparatus as described above is capable of arbitrarily setting a distance between the focal point of the laser beam and the substrate 7 to be

20     processed by the optical system shown in FIGs. 18 to 20 and adjusting an energy profile of the laser beam irradiated on the substrate 7 by setting the distance at a predetermined value as described below.

25     EXAMPLES

FIG. 21 is a graph of a first practical example, showing a beam profile with regard to the ELA apparatus shown in FIG. 18

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in a case in which a distance between a focal point of a laser beam and a substrate to be processed was set at $300\mu$m. In this graph, the energy level had a shape that spikes to the left side of the profile. FIGs. 22A, 22B, and 22C are optical microphotographs showing when scanning was performed in such a manner that a scan direction of a line beam with the energy profile shown in FIG. 21 was set in the left direction in FIG. 21. It is possible to examine a state of the film by observing interfered light, caused by a difference of a grain size, which had different color depending on grain size because of Secco etching performed. FIGs. 22A, 22B, and 22C correspond to energy densities of 390mJ/$cm^2$, 400mJ/$cm^2$, and 410mJ/$cm^2$ respectively. FIGs. 23A, 23B, and 23C are optical microphotographs taken when scanning is performed in such a manner that a scan direction of a line beam with the energy profile shown in FIG. 21 is set in the right direction. In FIGs. 22A, 22B, and 22C, there are very few black points in which defective crystallization regions exist and those that are present are not localized, showing a p-Si layer having excellent quality is formed. On the other hand, in FIGs. 23A, 23B, and 23C, vertically linear defective crystallization regions shown in black are recognized. Further, as shown in FIG. 23C, linear black regions are quite prominent, showing the existence of a large area of defective crystallization, and that the film is of a remarkably low quality.

The following can be inferred from the above observations. In the line beam having the energy profile shown in FIG. 21,

the jumping part is subject to exceed the microcrystallizing temperature or the threshold value energy Eth over which a grain size rapidly decreases. Especially, the more enhanced the laser energy is, the higher the probability that such event will occur. When the line beam was scanned in the right direction of FIG. 21, the film to be processed was annealed while the very end of irradiated region along the scan direction is microcrystallized. Accordingly, p-Si formed at the front area with respect to the scan direction was changed into microcrystal at the rear of the beam and remains as defective crystallization regions as shown in FIGs. 23A, 23B, and 23C. Such events are apt to occur with higher energies. Therefore, in attempts to obtain a large grain size, a problem occurs that microcrystal is formed.

On the contrary, when the line beam was scanned in the left direction of FIG. 21, microcrystal tended to form toward the front area of the beam. Thereafter, however, excellent crystallization was performed within the energy region just below the threshold value energy as the beam passes, thereby forming p-Si having a large grain size. In FIG. 22C, few defective crystallization regions in black are recognized, showing that the upper limit of the energy range to be set is less than 410mJ/cm$^2$.

Therefore, it is understood with the beam line having the energy profile as shown in FIG. 21 that an ideal annealing for crystallizing is performed in conditions that the energy of the beam is set at about 400 to 410mJ/cm$^2$ and a scan direction

30

is in the left direction of the figure.  In these conditions,
microcrystal is formed at the front area of the beam.
However, there is an area between the center area and the rear
area of the beam that the energy level shifts from an energy

5      region higher than the threshold value energy Eth over which a
grain size rapidly decreases to an energy region lower than
the threshold value energy Eth, thereby existing an optimal
beam region GR in which an ideal annealing is performed.  In
this example, the laser beam is scanned such that a total of

10     twenty pulses are performed.  Thus, the number of pulses
within the optimal beam region GR is less than twenty.
However, as shown in FIGs. 9, 10, and 15, the initial several
pulses complete formation of grains.  Accordingly, it is
possible to perform an excellent annealing by setting an

15     overlap amount and a pulse frequency to optimal values such
that an area in the film to be processed receives beam pulses
at predetermined times.

FIG. 24 is a graph, as a second example, showing a beam
profile with regard to the ELA apparatus shown in FIG. 18 in a

20     case where the distance between a focal point of a laser beam
and a substrate to be processed was set at $600 \mu m$.  Change of
the focal distance in this manner allows deformation of the
beam profile utilizing an infinitesimal gap in light caused by
diffraction and interference.  FIGs. 25A, 25B, and 25C are

25     optical microphotographs taken when scanning was performed in
such a manner that a scan direction of a line beam with the
energy profile shown in FIG. 24 was set in the left direction.

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FIGs. 26A, 26B, and 26C are optical microphotographs from the right direction. FIGs. 25A, 25B, and 25C, and, FIGs. 26A, 26B, and 26C correspond to energy densities of 390mJ/cm$^2$, 400mJ/cm$^2$, and 410mJ/cm$^2$, respectively. The crystalline states

5     shown in FIGs. 25A, 25B, 26A, and 26B, are excellent, while, those in FIGs. 25C and 26C, show a greater amount of defective crystallization regions. Especially, in FIG. 26C, defective crystallization regions formed are outstanding. It is inferred from this fact that the upper limit of the energy

10     range to be set is about 410mJ/cm$^2$. In the laser beam profile of this example, as shown in FIG. 24, the profile has a shape that it is relatively high in the right side of the profile. Accordingly, when scanning was performed in the left direction, microcrystal was formed toward the rear scanning

15     region of the laser beam, which shortened the period of annealling within the optimal beam region GR in which an excellent annealing is performed to just below the threshold value energy Eth, past which grain size rapidly decreases. In other words, an annealing period under such optimal condition

20     is shortened. Therefore, crystallization of microcrystal was not sufficient, which in turn led to the formation of defective crystallization regions as shown in FIG. 25C.

    On the other hand, when the line beam was scanned in the right direction, in the initial stage of the laser energy

25     irradiation, an annealing with an energy level over the threshold value energy Eth was performed. Thereafter, as in FIG. 7, since the period to be annealed within the optimal

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beam region GR in which an excellent annealing is performed just below the threshold value energy Eth is sufficiently long, a p-Si layer with an excellent crystallinity, as shown in FIGs. 26A to 26C, was obtained.

5      A third example follows.  In this example, a distance between a focal point of a laser beam and a substrate to be processed was set at $900 \mu m$.  FIG. 27 is a graph showing a beam profile in this case.  FIGs. 28A, 28B, 28C, 29A, 29B, and 29C are optical microphotographs taken when scanning was

10     performed in such a manner that a scan direction of a line beam with the energy profile shown in FIG. 27 was set in the left and the right directions, respectively.  FIGs. 28A, 28B, and 28C, and FIGs. 29A, 29B, and 29C correspond to energy densities of $390 mJ/cm^2$, $400 mJ/cm^2$, and $410 mJ/cm^2$ respectively,

15     as was the case for the previous examples.  In all of these FIGs. 28A to 29C, the crystalline state is excellent.  In the laser beam profile shown in FIG. 27, the profile has a shape, similar to FIG. 8, where a portion of the graph peaks in energy to the right of the center area of the profile, and the

20     energy level gently decreases at both sides of the peak. Accordingly, regardless of the scan direction, which may be either the left direction or the right direction, the optimal beam region GR, in which a sufficiently large grain size can be obtained, exists at an energy level shifting from a region

25     higher than the threshold value energy Eth to a region lower than the threshold value energy Eth, thereby enabling excellent annealing to be performed.

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Finally, a construction example in which a transistor device, specifically a thin film transistor, was formed utilizing a polycrystal silicon film obtained by the above-described laser annealing method will be explained.

5          FIG. 30 is a plane view of a TFT formed on the substrate 7 to be processed shown in FIG. 4 according to the present invention.  A p-Si layer formed by the ELA method according to the present invention was etched into an island-like shape for use in a TFT.  In the p-Si 11 thus formed, a non-doped channel
10        region Ch, light-doped regions LD, and heavy-doped source and drain regions S and D were formed.  On the channel region CH, a gate electrode 13 was formed with a gate insulating film inserted between the channel region and the gate electrode 13.

          FIG. 31 shows an example of a cross-section where a TFT is
15        completed.  A p-Si layer 31 is formed in an island-like shape on a non-alkaline glass substrate 7 as a substrate to be processed, a non-doped channel region CH is formed in the p-Si layer 31, and regions LD are formed in both sides of a non-doped channel region CH.  Source and drain regions S and D are
20        formed outside the regions LD.  A gate insulating film 12 covers the p-Si layer 31, and a gate electrode 13 consisting of a doped p-Si layer 13p, tungsten silicide 13s, or the like is formed at a region corresponding to the channel region CH.  An implantation stopper 14 for preventing counter-doping when
25        implantation ions of a different conductive type in the CMOS structure is formed on the gate electrode 13.  Side walls 15 of the gate electrode 13 are formed to previously prepare

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margins so that the regions LD might not be enhanced over the edges of the gate electrode 13 when impurities implanted into the p-Si layer 31 are diffused in the lateral direction by activation annealing. A first inter-layer insulating film 16

5      is formed so as to cover the entire surface of the substrate 7, and drain and source electrodes 17 and 18 made of low-resistance metal are formed on the first inter-layer insulating film 16 and are respectively connected with drain and source regions D and S through contact holes CT formed in

10     the gate insulating film 12 and the inter-layer insulating film 16.

If a TFT as shown in FIGs. 30 and 31 is used and constructed in a CMOS structure which is used as a driver circuit section (including a gate driver 23 and a drain driver

15     24) for an LCD as shown in FIG. 4, it is possible to simultaneously form a driver circuit with high performance and high speed in manufacturing steps substantially equal to those for a TFT for driving liquid crystal.

Further, in the display area 22 of the LCD shown in FIG.

20     4, a second inter-layer insulating film 19 having a flattening effect is formed on the entire surface so as to cover the drain electrode 17 and the source electrode 18 formed as shown in FIG. 32. In addition, a pixel electrode for driving liquid crystal is formed on the second inter-layer insulating film 19

25     and is connected with the source electrode 18.

For forming a liquid crystal display, another substrate is provided so as to face the substrate 7 on which TFTs and pixel

35

electrodes connected thereto are formed. A liquid crystal layer is formed between the substrate. A common electrode coupled with a pixel electrode to constitute a liquid crystal drive capacitor is formed on the substrate facing the

5    substrate 7.

As has been described above, by forming a polycrystal silicon film having a large grain size by an suitable laser annealing and utilizing the polycrystal silicon in a thin film silicon used for various devices (for example, a liquid

10    crystal display), it_is possible to form a transistor with a excellent operating characteristics by a low temperature process.

While there have been described what are at present considered to be preferred embodiments of the invention, it

15    will be understood that various modifications may be made thereto, and it is intended that the appended claims cover all such modifications as fall within the true spirit and scope of the invention.

20

WHAT IS CLAIMED IS:

1.  A semiconductor layer laser annealling method for improving characteristic of a semiconductor layer formed on a substrate by irradiating a laser beam, wherein

an energy level in a region to be irradiated by the laser beam is set such that a level towards the rear of a region along which the laser beam scans is lower than that at the front area or the center area of the region.

2.  A semiconductor layer laser annealling method for obtaining a polycrystal semiconductor layer by irradiating a laser beam on an amorphous semiconductor layer formed on a substrate, wherein

an energy level in a region to be irradiated by the laser beam is set such that a.level towards the rear of a region along which the laser beam scans is lower than that at the front area or the center area of the region.

3.  A laser annealling method according to claim 2, wherein the energy level at the front or center of the region is equal to or greater than the upper limit energy level, which thereby maximizes grain size of the semiconductor layer.

4.  A semiconductor layer laser annealling method for obtaining a polycrystal semiconductor layer by irradiation of an amorphous semiconductor layer formed on a substrate with a

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laser beam, wherein

an energy level in a region to be irradiated by the laser
beam is set such that the peak level in the rear area of a
region along a scan direction of the laser beam is lower than
5    the upper limit energy level which maximizes semiconductor
layer grain size.


5.    A laser annealling method according to claim 4, wherein
the peak level of the laser beam at the front area or the
10    center area of the region along the scan direction of the
laser beam is equal to or greater than the upper limit energy
level which maximizes a grain size of the semiconductor layer.


6.    A laser annealling method according to claim 4, wherein
15    the laser beam irradiated on the amorphous semiconductor layer
is obtained by shaping a laser beam generated from a laser
oscillation source by an optical system including a plurality
of lenses, such that the region to be irradiated has a
predetermined shape, and

20    the energy level, energy distribution, or their
combination in the region to be irradiated by the laser beam
are controlled by adjusting a distance between the amorphous
semiconductor layer formed on the substrate and the focal
point of the laser beam formed by the optical system.

25

7.    A laser annealling method according to claim 6, wherein
the scan direction of the laser beam is set such that an

energy level at the rear area of the region along the scan direction is lower than the upper limit energy level.

8.   A laser annealling method according to claim 4, wherein
5    the upper limit energy level which maximizes a grain size of the semiconductor layer corresponds to the lower limit energy level over which the polycrystal semiconductor layer is changed into an amorphous state.

10   9.   A transistor device in which a polycrystal semiconductor layer is formed by subjecting an amorphous semiconductor layer formed on a substrate to laser anneal processing, wherein
     an energy level in a region to be irradiated by a laser beam of the amorphous semiconductor layer is set such that the
15   level in a rear area of a region along a scan direction of the laser beam is lower than the upper limit energy level which maximizes a grain size of the semiconductor layer, and
     the amorphous semiconductor layer is annealed by the laser beam and the polycrystal semiconductor layer obtained is used
20   as an active layer of the transistor device.

10.  A transistor device according to claim 9, wherein
     the transistor device is a thin film transistor, and
     a channel layer of the thin film transistor is formed in
25   the polycrystal semiconductor layer obtained by the laser anneal processing.

11. A transistor device according to claim 9, wherein

the transistor device is a thin film transistor,

a channel layer of the thin film transistor is formed in

the polycrystal semiconductor layer obtained by the laser

5    anneal processing, and

the thin film transistor is used as a switching device

formed in a display area of a substrate forming a liquid

crystal display and as a switching device of a driver circuit

formed surrounding the display area of the substrate through a

10    process substantially equal to a process of forming the

switching device of the display region.

15

## ABSTRACT

For obtaining p-Si by irradiating a laser beam to an a-Si
layer to polycrystallize, an energy level in a region to be
5    irradiated by the laser beam is set such that a level at the
rear area of the region along a scan direction of the laser
beam is lower than that at the front area or the center area
of the region. The energy level at the front area or the
center area of the region is set such that it is substantially
10   equal to or more than the upper limit energy level which
maximizes a grain size of the p-Si obtained. Since an energy
profile is set as described above, when the laser beam is
scanned on the a-Si layer, an irradiated energy of the laser
on the region is gradually lowered from the upper limit as the
15   laser beam passes through, which allows the semiconductor
layer to be annealed within an optimal energy level during the
latter half of the annealing process.

**Fig. 1  PRIOR ART**

GATE LINE



**Fig. 2**



**Fig. 3**

**7**

**24**

**22**

**23**

**24**

**25**

C

# Fig. 4

SCAN DIRECTION

GR

Eth

ENERGY

POSITION

**Fig. 5**

SCAN DIRECTION

Eth

ENERGY

GR

POSITION

**Fig. 6**

SCAN DIRECTION

GR

Eth

ENERGY

POSITION

**Fig. 7**

SCAN DIRECTION

GR

Eth

ENERGY

POSITION
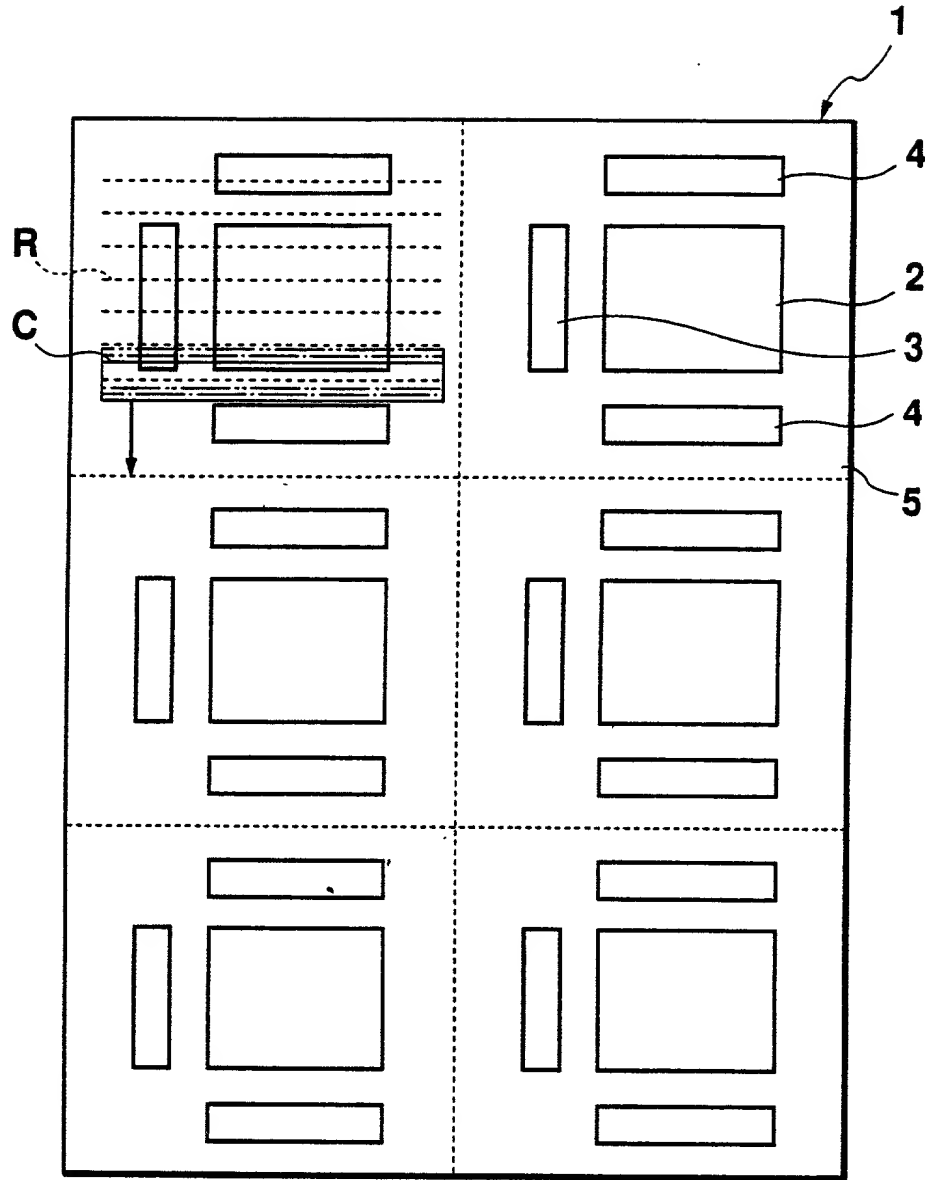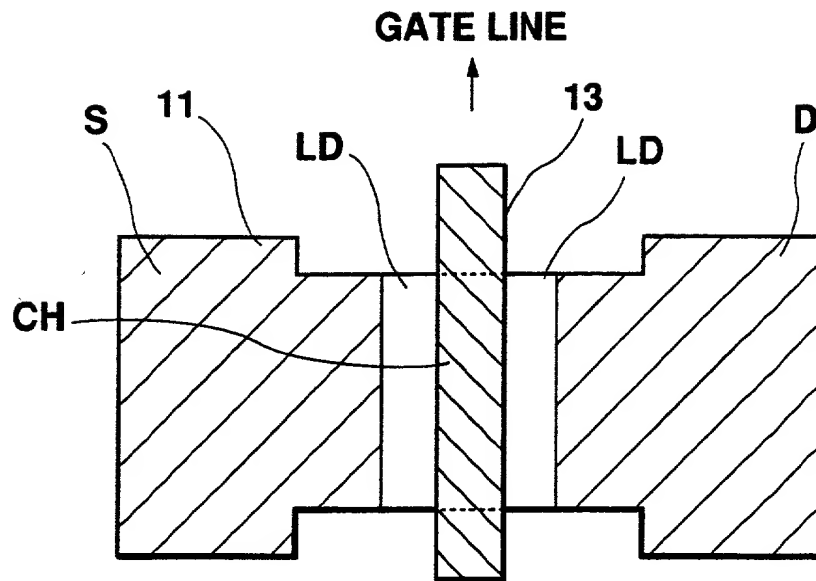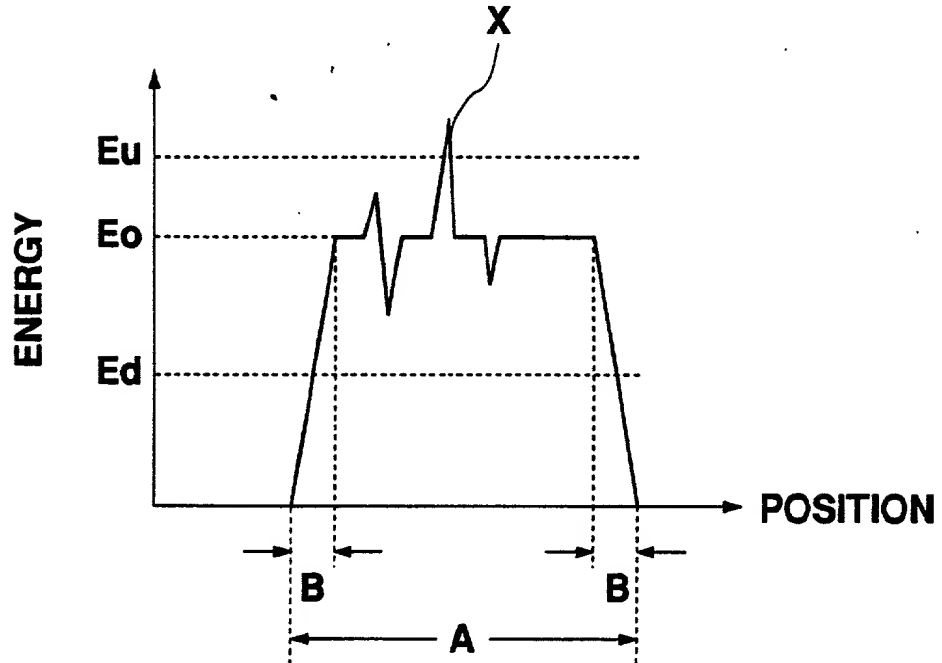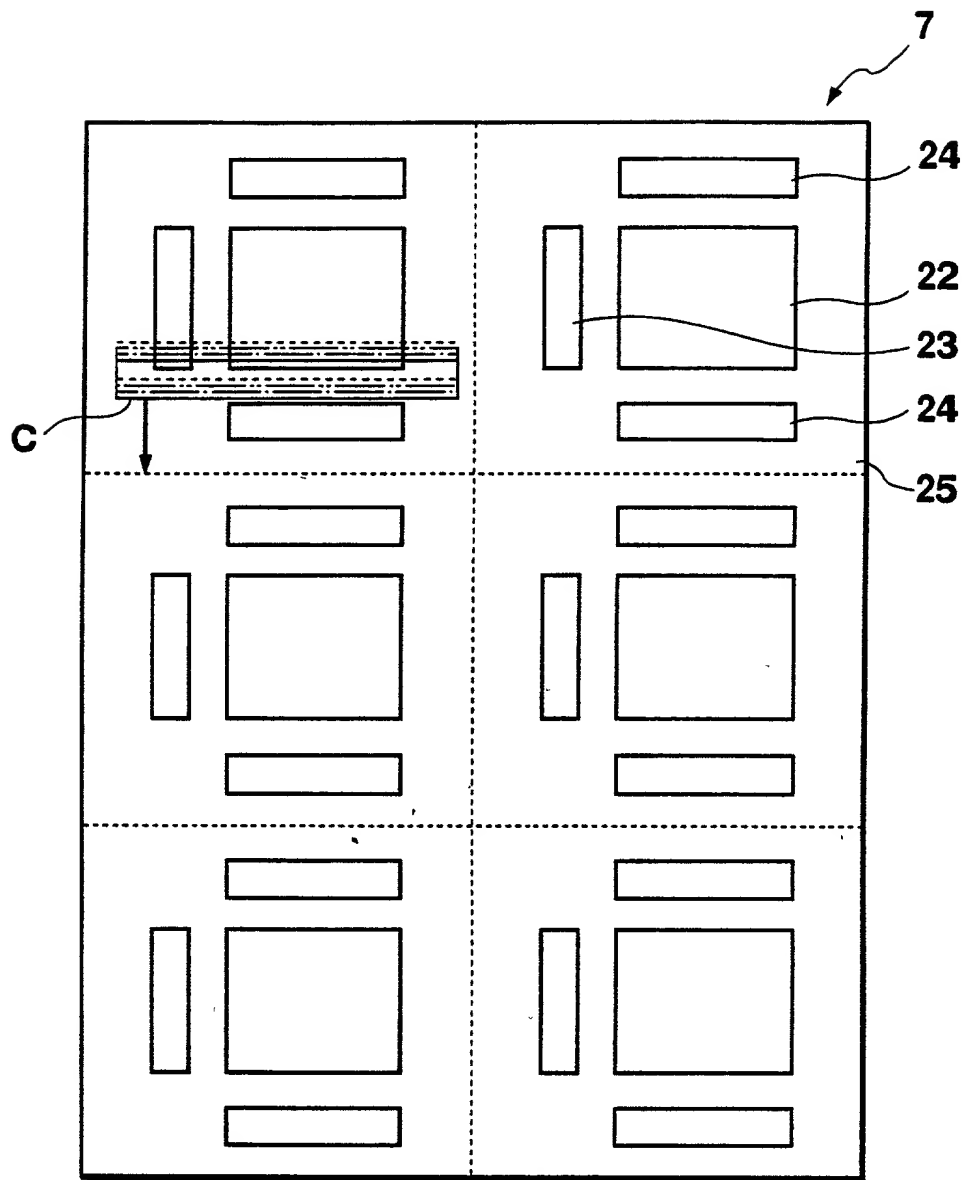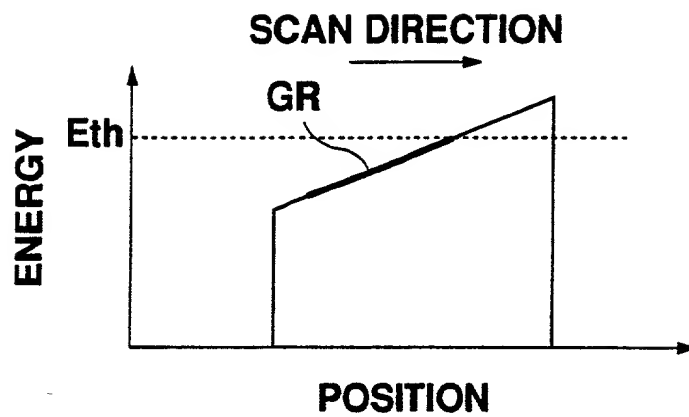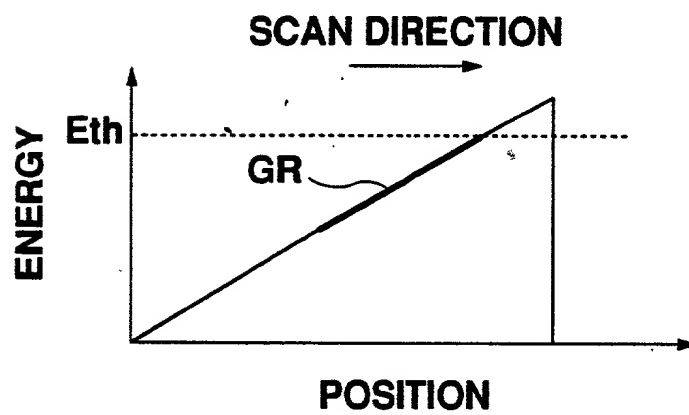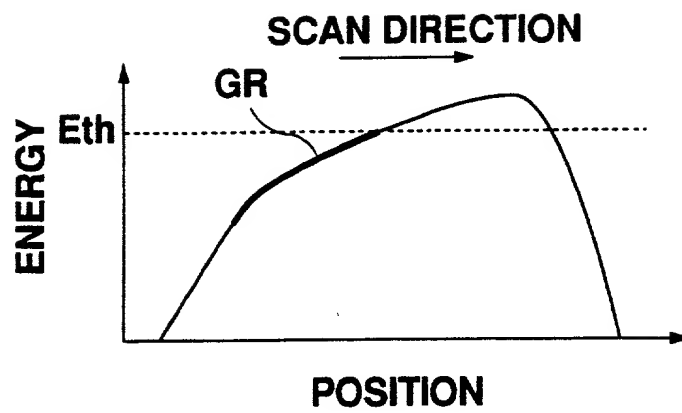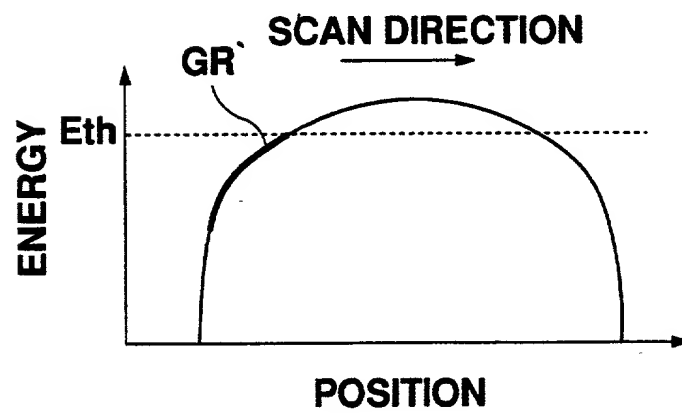
**Fig. 8**

TEMPERATURE



Fig. 9



Fig. 10

Fig. 11

MX

TM

Tg

p-Si          M-cry          p-Si    a-Si



GRAIN SIZE

GM

Gg

20 PULSES          1 PULSE

POSITION

## Fig. 12

×125

×125

40μm

40

Fig. 13A

20μm

20μm

20μm

20μm

×25

×25

Fig. 13B    ×250

Fig. 13C    ×250

**Fig. 14**

**Fig. 15**

×125

×125

40μm

40μm

## Fig. 16A

20μm

×250

20μm

×250

20μm

×250

20μm

×250

×250

## Fig. 16B

## Fig. 16C

**Fig. 17**

FOCUS POINT-SUBSTRATE 300μm
BEAM SCAN DIRECTION



**Fig. 21**

Fig. 18

58   59   62   63   60   7

**Fig. 19**

A

57   65   7

**Fig. 20**

Fig. 22A

390mJ/cm²

Fig. 22B

400mJ/cm²
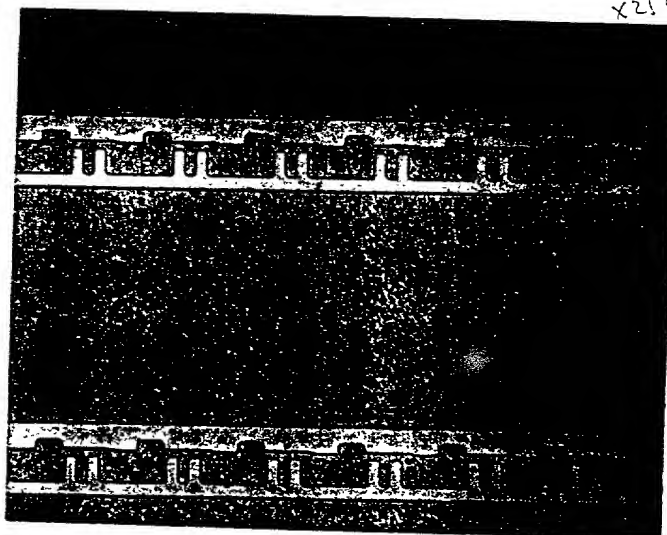
Fig. 22C
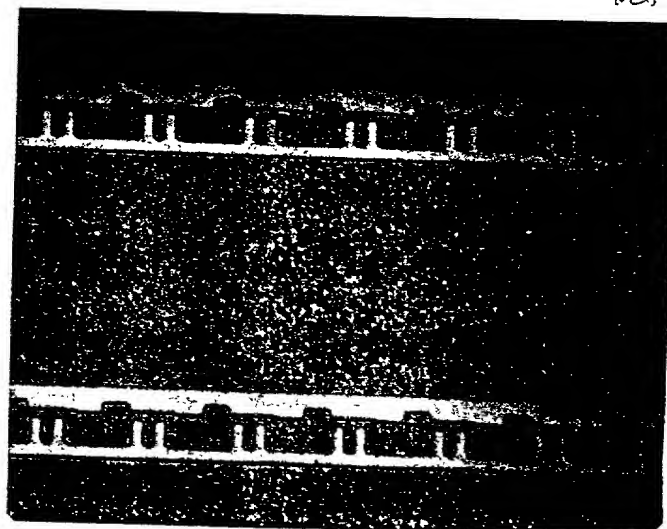
×250



Fig. 23A

390mJ/cm²

×250



Fig. 23B

400mJ/cm²

×250



Fig. 23C

410mJ/cm²
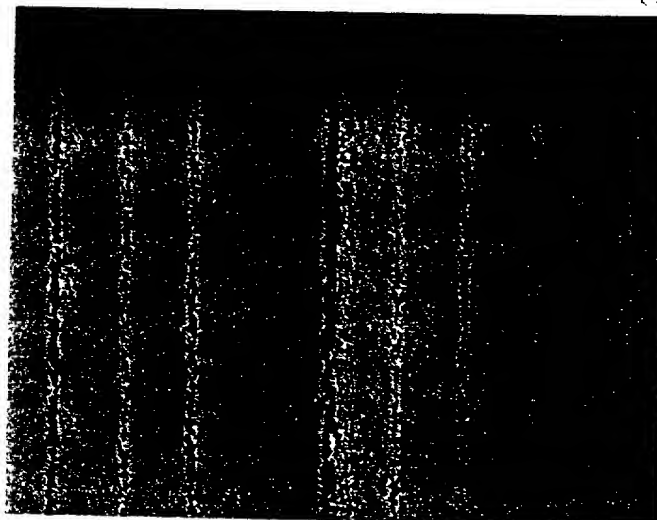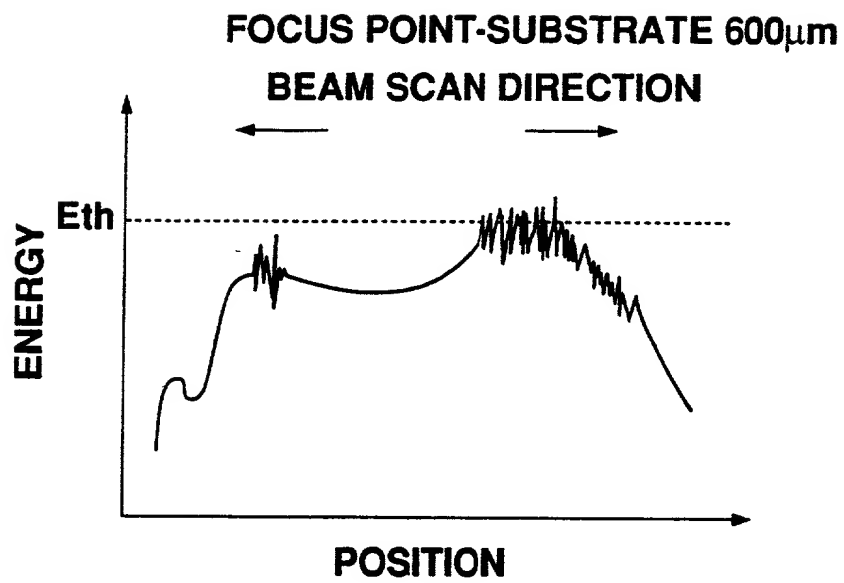
FOCUS POINT-SUBSTRATE 600μm
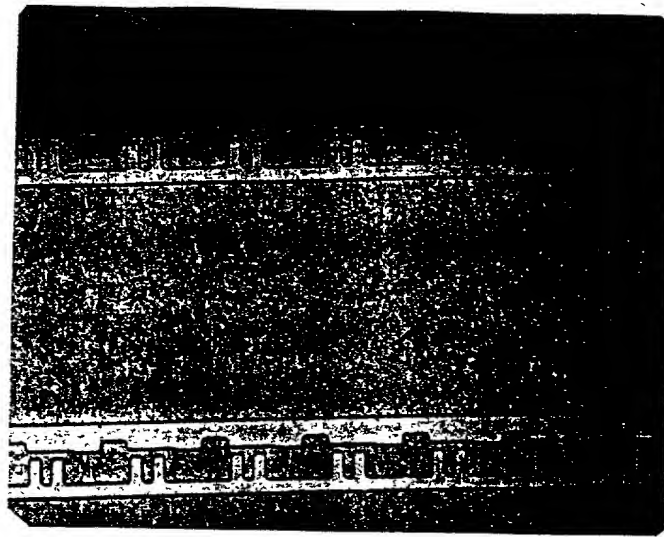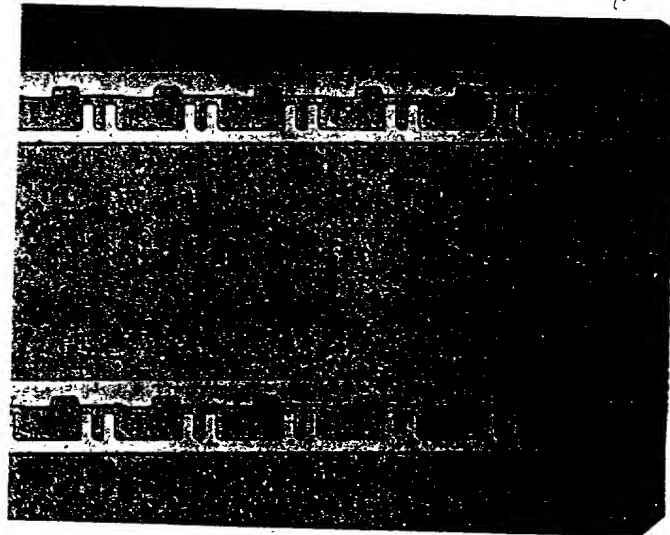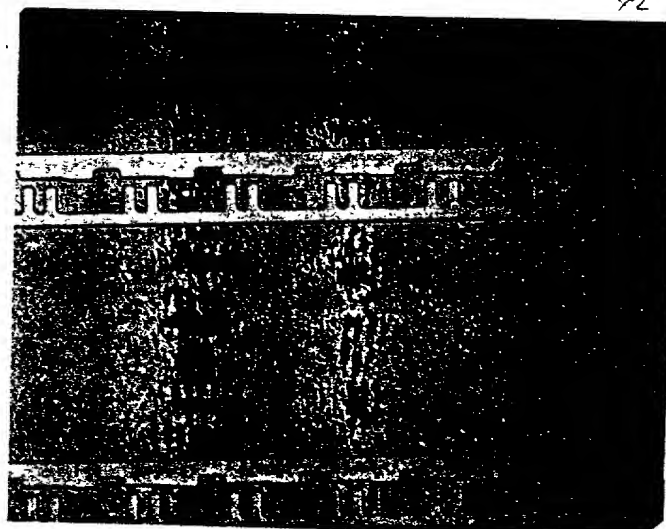
BEAM SCAN DIRECTION



**Fig. 24**

Fig. 25A

×250

390mJ/cm²

Fig. 25B

×250

400mJ/cm²

Fig. 25C

×250

Fig. 26A



390mJ/cm²

×250

Fig. 26B



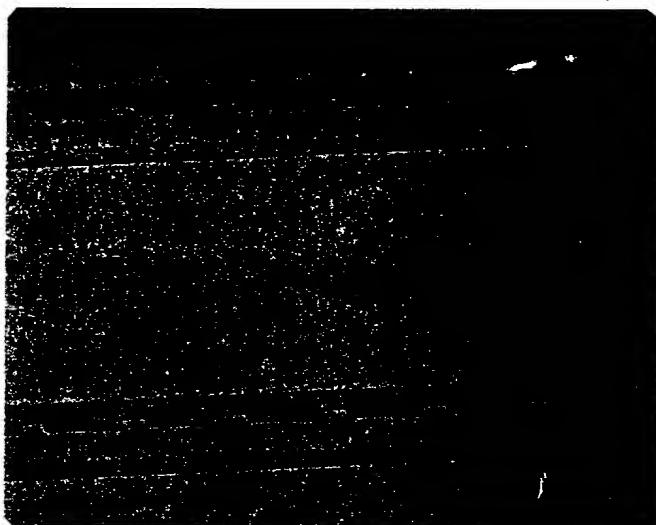400mJ/cm²

×250

Fig. 26C
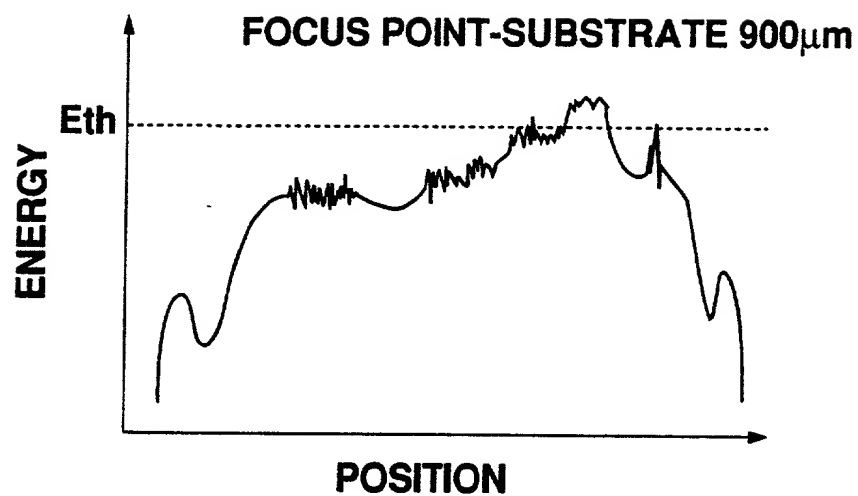


410mJ/cm²
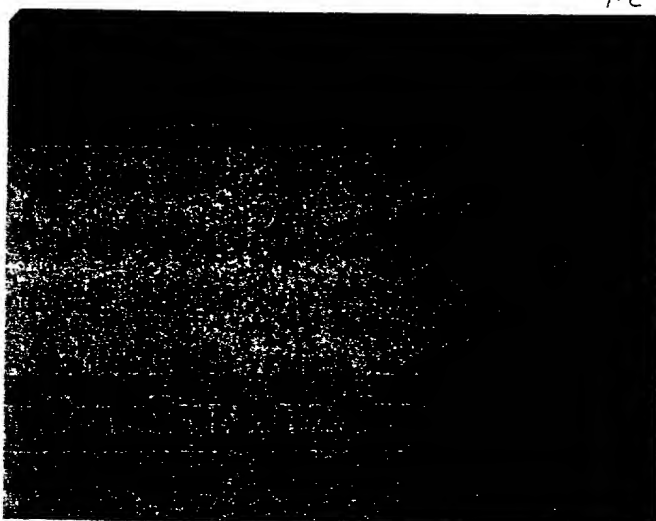
Fig. 27

×250
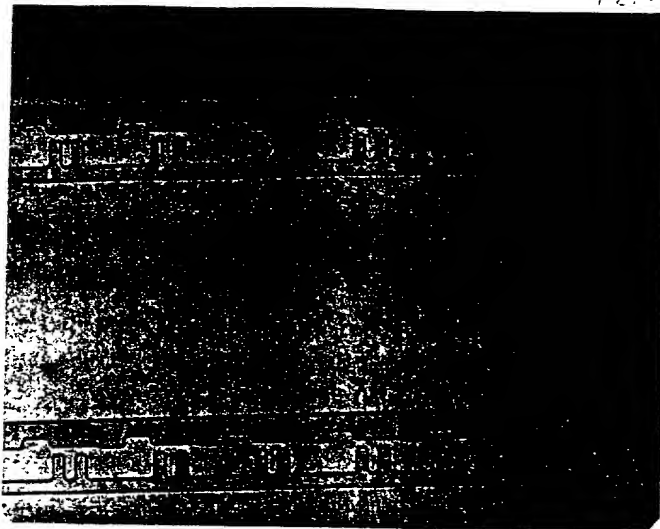
Fig. 28A

390mJ/cm²



×250

Fig. 28B

400mJ/cm²



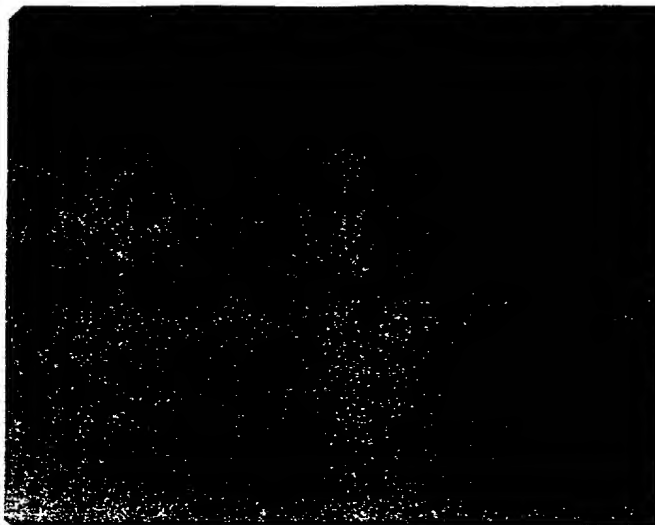×250

Fig. 28C

×250

Fig. 29A

390mJ/cm²
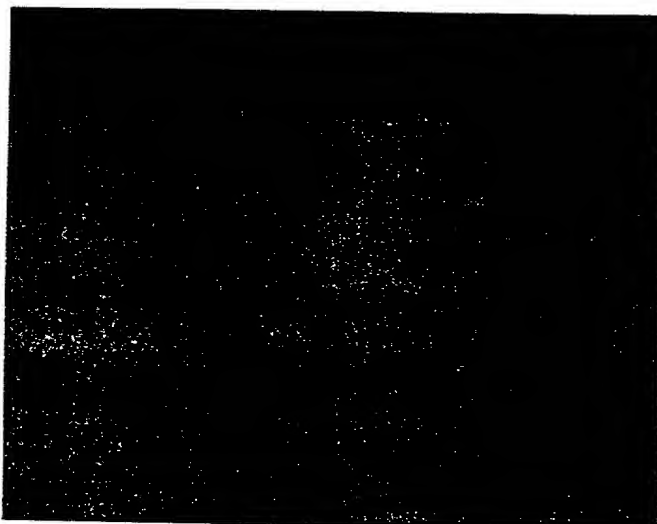


×25.0

Fig. 29B
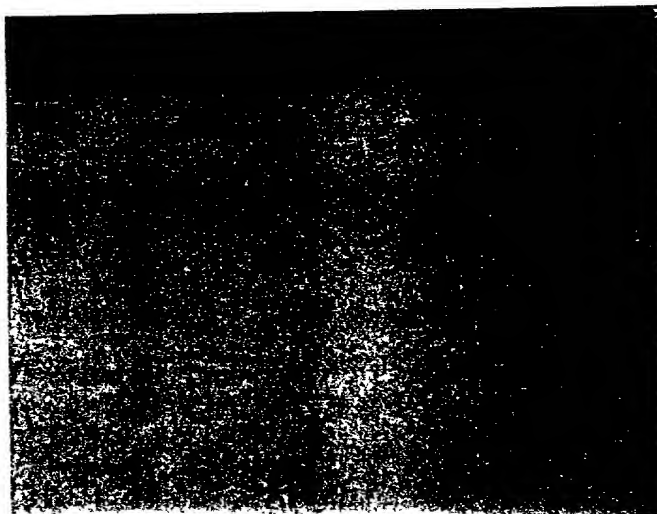
400mJ/cm²



×250

Fig. 29C
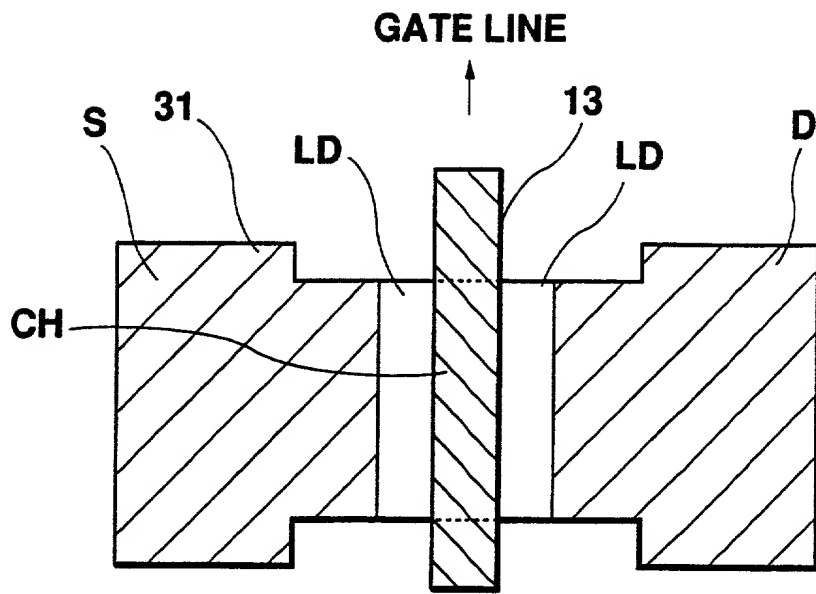
GATE LINE
↑

S    31    LD    13    LD    D

CH

**Fig. 30**

14
15    13p 13s
17    15    18
16    31
12
7

D    LD    CH    S

**Fig. 31**

SUB-STRATE

COMMON
ELECTRODE

LC
LAYER

14

17

18

19

PIXEL
ELECTRODE

16

12

7

D

13s

13p

CH

LD

S

15

15

TFT

**Fig. 32**

PATENT (U S.A.)

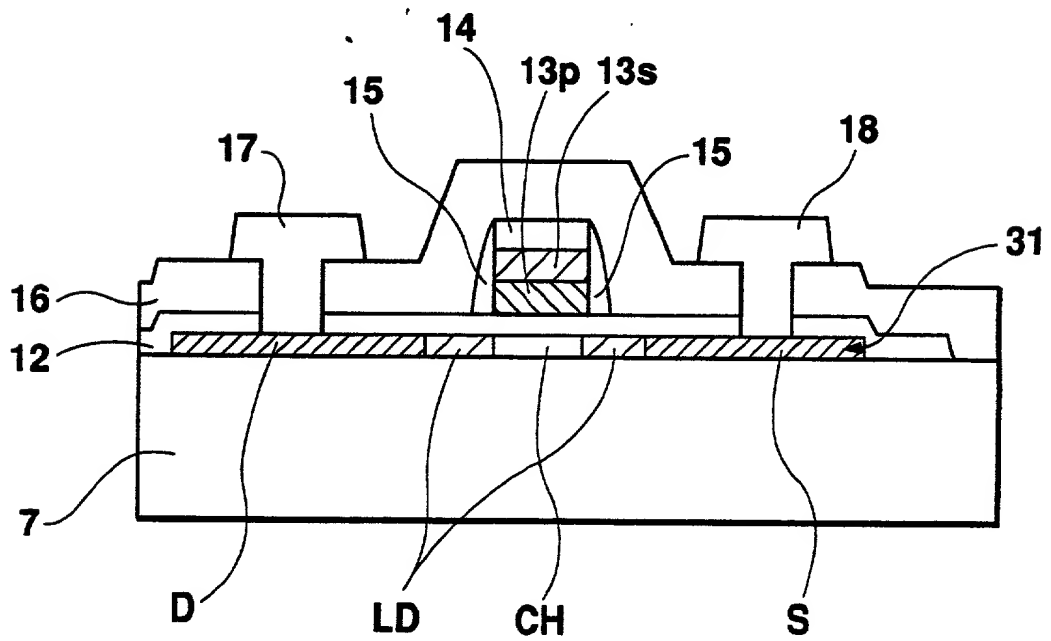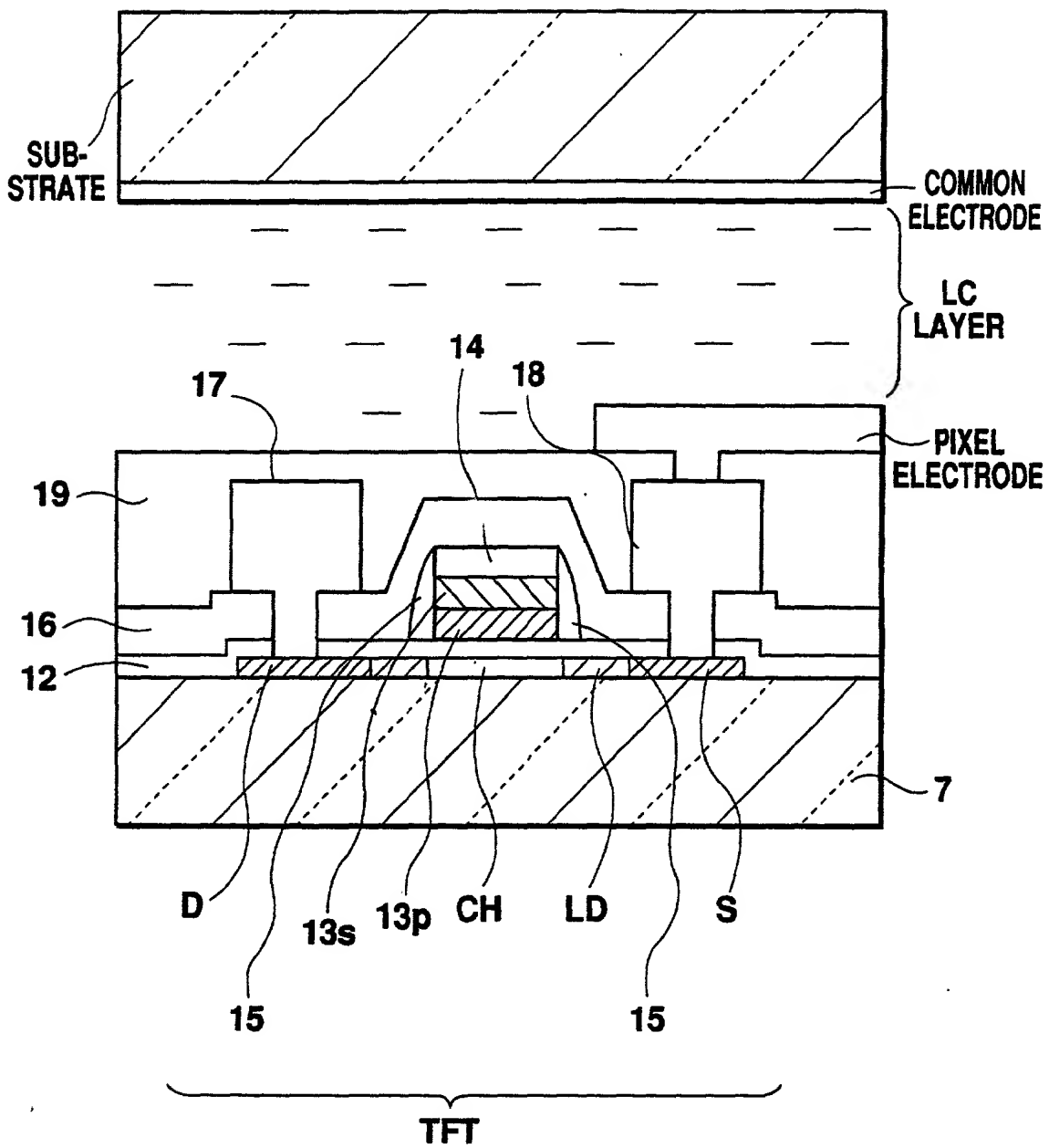ATTORNEY'S DOCKET NO _____

**DECLARATION**
**and POWER OF ATTORNEY**

5586/PD-5827

☐ ORIGINAL
☐ CONTINUATION
☐ DIVISIONAL

As a below named inventor, I declare that the information given herein is true, that I believe that I am the original, first and sole inventor if only one name is listed at 1 below, or a joint inventor if plural inventors are named below at 1-4, for the invention entitled:

## LASER ANNEAL METHOD OF A SEMICONDUCTOR LAYER

Which is described and claimed in:

☒ the attached specification or

☐ the specification in application Serial No. _____ filed _____

☐ as amended on _____ (for declaration not accompanying application, if applicable)

and for which a patent is sought, and that my residence, post office address and citizenship are as stated below next to my name.
I acknowledge my duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations §1 56(a)
I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

| COUNTRY | APPLICATION NUMBER | DATE OF FILING Month Day Year | PRIORITY CLAIMED UNDER 35 U.S.C. 119 |
|---|---|---|---|
| Japan | Hei 8-217424 | August 19, 1996 | YES X NO ___ |
| | | | YES ___ NO ___ |

I hereby claim the benefit under Title 35, United States Code, §1120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

| (Application Serial No.) | (Filing Date) | (Status) |
|---|---|---|

**POWER OF ATTORNEY:**
As a named Inventor, I hereby appoint the following attorney(s) and/or Agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: STUART LUBITZ, Reg. No. 20,680; RICHARD H. ZAITLEN, Reg. No. 27,248; ALEX CHARTOVE, Reg. No. 31,942; DAVID M. SIMON, Reg. No. 32,756; JAY M. FINKELSTEIN, Reg. No. 21,082; ROGER R. WISE, Reg. No. 31,204; GARY D. MANN, Reg. No. 34,867; DON F LIVORNESE, Reg. No. 32,040; WILLIAM K KONRAD, Reg. No. 28,868; LOUIS A. MOK, Reg. No. 22,585; JOHN P. SCHERLACHER, Reg. No. 23,009; TED R RITTMASTER, Reg. No. 32,933; SAMUEL L. ALBERSTADT, Reg. No. 32,766; PAUL H. KOVELMAN, Reg. No. 35,228, PAUL G. NAGY, Reg. No. 37,896, JONATHAN Y. KANG, Reg No. 38,199; DAVID L. LUBITZ, Reg. No. 38,229; MARGARET A. KIVINSKI, Reg. No. 38,517; WEINING YANG, Reg. No 38,690; ALAN S. RAYNES, Reg. No. 39,809, DAVID W VICTOR, Reg. No. 39,867; CHRIS P. PERQUE, Reg. No. 37,696; PHILIPPE O. ERWIN, Reg. No 38,132; RANDALL C. FURLONG, Reg. No. 35,144; and JOSEPH F. VONSAUERS, Reg. No. 37,253.

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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

| SIGNATURE OF INVENTOR 1 *Hidenori Ogata* | SIGNATURE OF INVENTOR 2 *Ken Wakita* |
|---|---|
| DATE: August 8, 1997 | DATE: August 8, 1997 |
| SIGNATURE OF INVENTOR 3 *Kiyoshi Yoneda* | SIGNATURE OF INVENTOR 4 *Yoshihiro Morimoto* |
| DATE: August 8, 1997 | DATE: August 8, 1997 |

# DECLARATION
## and POWER OF ATTORNEY

### PRIOR FOREIGN APPLICATION(S)

| COUNTRY | APPLICATION NUMBER | DATE OF FILING Month Day Year | PRIORITY CLAIMED UNDER 35 U.S.C. 119 |
|---------|--------------------|-------------------------------|--------------------------------------|
|         |                    |                               | YES __ NO __ |
|         |                    |                               | YES __ NO __ |
|         |                    |                               | YES __ NO __ |

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We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

| SIGNATURE OF INVENTOR 5 *Tsutomu Yamada* | SIGNATURE OF INVENTOR 6 *Kazuhiro Imao* |
|---|---|
| DATE August 8, 1997 | DATE August 8, 1997 |
| SIGNATURE OF INVENTOR 7 *Takashi Kuwahara* | |
| DATE August 8, 1997 | |